ST-NXP Wireless

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- **Web site** - http://www.st.com is replaced with http://www.stnwireless.com
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ST-NXP Wireless

STn8811A12

Mobile multimedia application processor

Data Brief

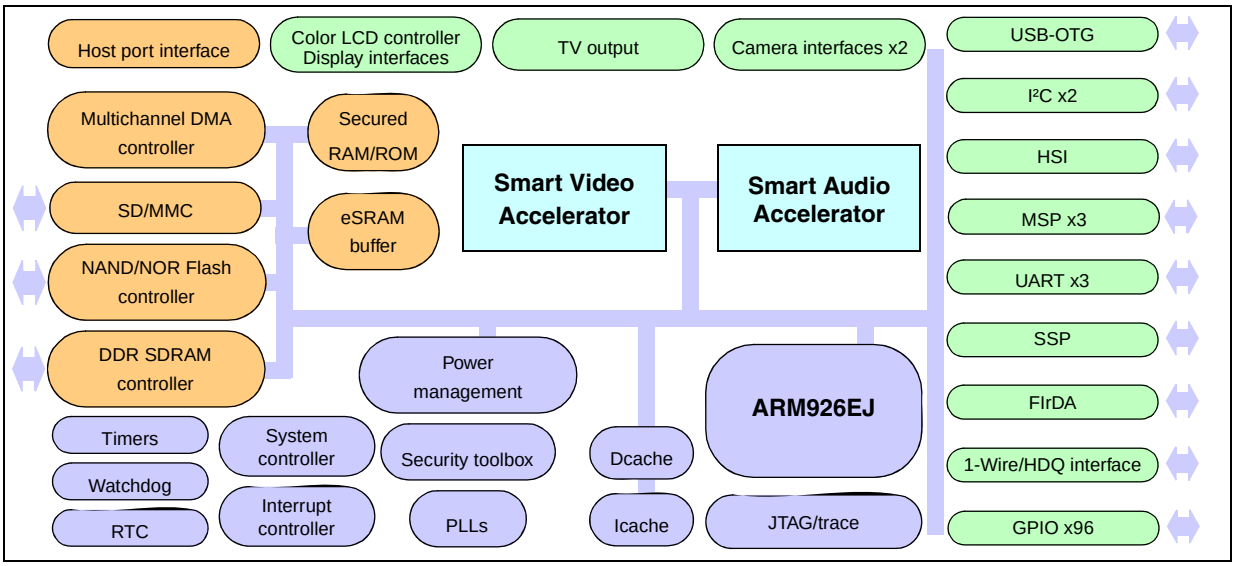
Nomadik is a registered trademark of STMicroelectronics

Features

- ARM926EJ at 393 MHz
  - 32-Kbyte instruction/16-Kbyte data caches
- Audio and video accelerated processing; all ARM MIPs available for user applications
- Video performance
  - Real-time MPEG4 Simple Profile encoding or decoding, up to VGA 30fps
  - WM9/VC-1 encode/decode support
  - H.264 encode/decode support - QVGA 30 fps decode
  - JPEG encode or decode, up to 4080 x 4080 pixels
- Audio performance
  - Extensive digital-audio software library
  - Optimized for low power on SAA
- Camera interfaces
  - Serial interface up to 416 Mbit/s (MIPI legacy CSI)
  - Parallel camera CCIR-656 interface up to 66 MHz (MIPI legacy CPI)
- Color LCD controller
- TV output
- Advanced power management unit
- Advanced security
  - Comprehensive security framework
  - Protected access to secured ROM and RAM
- 16-bit DDR/SDR-SDRAM memory controller
- NOR Flash/NAND Flash/Compact Flash/CF+ controller
- MultiMediaCard/SD Card host controller
- Full set of IO peripherals
- TFBGA 12mm x 12mm x 1.2mm, 0.5 mm pitch

Description

The STn8811A12 application processor enables smart phones, mobile multimedia consumer like PMP, PND, internet appliances and in-car entertainment systems to play back media content, record pictures and video clips, receive mobile-TV and perform video conference.



1 STn8811A12 overview

1.1 Features

- Smart video accelerator
  - Real-time MPEG4 Simple Profile encoding or decoding, up to VGA 30fps
  - JPEG encode or decode, up to 4080 x 4080 pixels
  - Ultra low-power implementation
- Smart audio accelerator
  - Extensive software library including AAC+, SBC, G711, G729,and more
  - Ultra low-power implementation
- Camera interfaces
  - Supports high-resolution sensors up to 4 Megapixels
  - Serial interface up to 416 Mbit/s (MIPI legacy CSI)
  - Parallel camera CCIR-656 interface up to 66 MHz (MIPI legacy CPI)
- TV output
- Advanced power management unit
  - Run, idle, doze and sleep modes
  - CPU clock with programmable frequency
  - Embedded 1.2 V logic supply switch
- ARM926EJ 32-bit RISC CPU, at 393 MHz
  - 32-Kbyte instruction cache, 16-Kbyte data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, byte Java mode (Jazelle™) for direct execution of Java code
  - Embedded medium trace module (ETM Medium+)
- On-chip SRAM: 40 Kbytes + 16 Kbytes with secured access + 1 Kbyte backup
- On-chip ROM: 32 Kbytes for boot + 64 Kbytes with secured access
- Advanced security
  - Comprehensive security framework
  - Protected access to secured ROM and RAM
- 16-bit DDR/SDR-SDRAM memory controller
- NOR Flash/NAND Flash/Compact Flash/CF+ controller
- MultiMediaCard/SD Card host controller
- Color LCD controller for STN or TFT panels or display interface for display module
  - 24-bpp true color
  - MIPI legacy DBI and DPI
- USB On-The-Go interface up to 12 Mbit/s
- Host port interface
- I/O peripherals
  - 3 autobaud UARTs (one with modem control signals) up to 3.692 Mbit/s
  - One IrDA (SIR/MIR/FIR) interface up to 4 Mbit/s

  - One synchronous serial port (SSP) up to 24 Mbit/s
  - 3 multichannel serial ports (MSP) up to 48 Mbit/s
  - Two I²C multi-master/slave interfaces
  - One 8-channel, full-duplex high-speed serial interface, 108 Mbit/s
  - 1-Wire®/HDQ interface [a]
- 96 general-purpose I/Os (muxed with peripheral I/Os)
- System and peripheral controller
  - Multichannel DMA controller
  - 32-source interrupt controller
  - Eight 32-bit timers/counters
  - Real-time clock (RTC)
  - Real-time timer (RTT)
  - Watchdog timer
- Programmable PLL for CPU and system clocks
- 13/19.2 MHz crystal oscillator
- JTAG IEEE 1149.1 boundary scan
- Supply voltages
  - 1.45 V nominal, 1.2 V logic; 1.8 V to 2.5 V I/O, PLL analog; 2.5 V OTP
- TFBGA 12mm x 12mm x 1.2mm, 288 + 36 balls, 0.5 mm pitch

1.2 General description

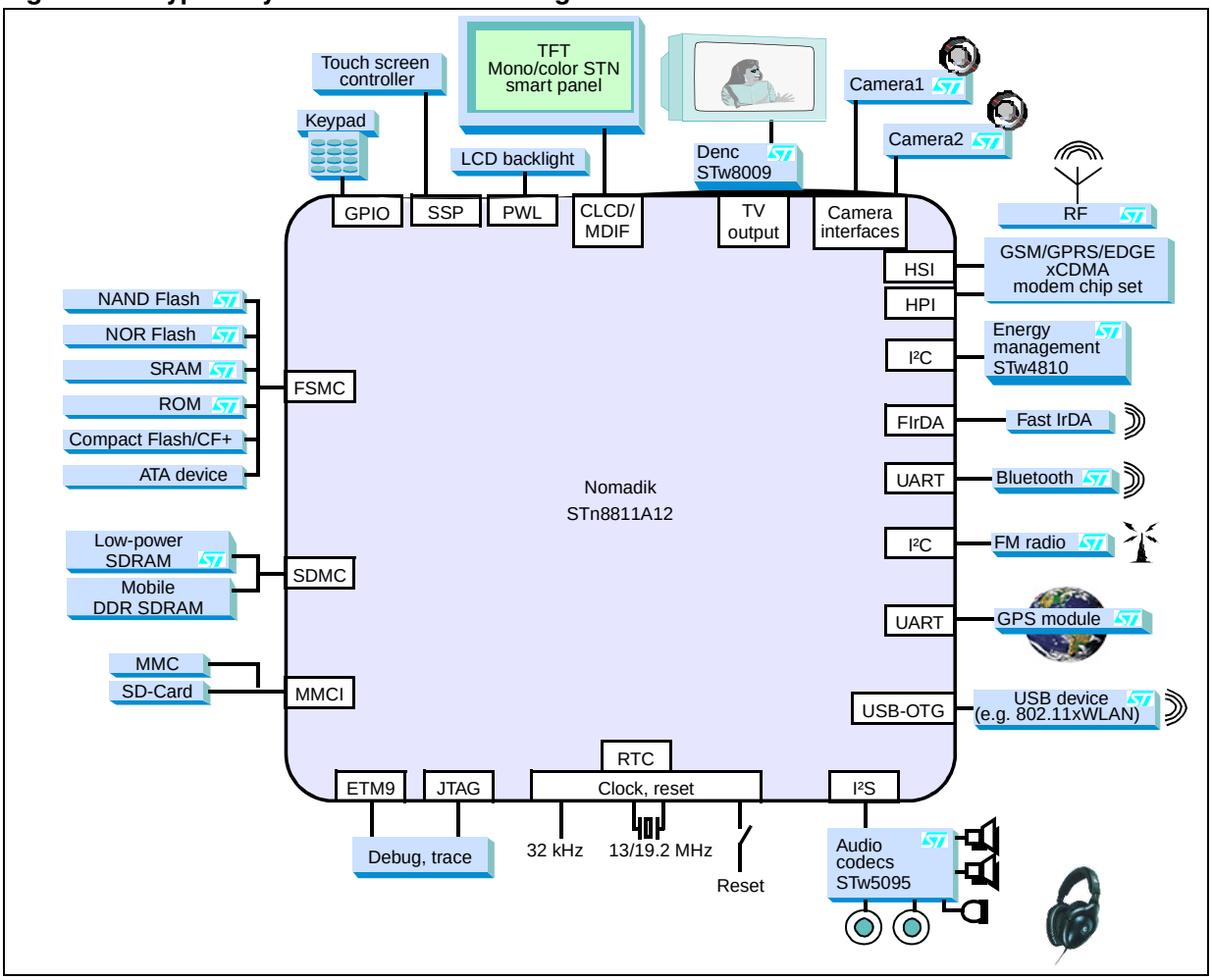
The convergence of computing, multimedia and mobile communications is well underway. The familiar voice phone is being transformed into a personal device with a wide range of multimedia capabilities including capturing, sending and receiving images, videos and music. To deliver such data-heavy, processing-intensive services, portable handheld systems must be optimized for performance and low power, space and cost.

In response to this need, the STn8811A12 processor platform from STMicroelectronics is a culmination of breakthroughs in video coding efficiency, inventive algorithms and chip implementation schemes. It will enable smart phones, portable media players, portable navigation devices, internet appliances and car entertainment systems to play back media content, record pictures and video clips, receive mobile-TV and perform bidirectional audio-visual communication with other systems in real time.

The STn8811A12 focuses on the essential features to meet the future needs of mobile products and services: a high-performance multimedia capability coupled with low power consumption, and based on an open platform strategy.

a. 1-Wire is a registered trademark of Dallas Semiconductor

Figure 1. Typical system architecture using the STn8811A12



1.3 Key benefits

The STn8811A12 brings the following key benefits to mobile manufacturers and consumers:

- unsurpassed audio and video quality
- ultra-low power consumption for longer battery operation
- easier application development for shorter time-to-market
- scalability for multiple market segments and future multimedia applications

1.4 Main features

The STn8811A12 processor platform enables compelling multimedia applications by means of its unique distributed-processing architecture. The application processor features low-power smart accelerators which handle all audio and video functions. These free the main CPU for control and program flow tasks, or allow the CPU to enter power-saving modes to prolong battery life. The smart accelerators operate independently and concurrently to ensure the lowest absolute system power and deterministic high-performance.

The main features of the platform are:

- A smart video accelerator for VGA video encoding and decoding, with MIPI camera interfaces.
- A smart audio accelerator containing a comprehensive set of digital audio decoders and encoders, and offering a large number of 3-D surround effects.
- An advanced power management unit which offers a number of power saving modes.
- The ARM926EJ processor, a powerful industry-standard CPU with Java acceleration.
- On-chip ROM and SRAM memory devices.
- Advanced security framework for authentication and digital rights management.
- Multichannel DMA controller for efficient data transfer without CPU intervention.
- A multi-layer AMBA crossbar interconnect for optimized data transfers between the CPU, accelerators, memory devices and peripherals.
- A wide range of peripheral interfaces (GPIO, USB-OTG, UART, I²C, FIrDA, SD/MMC, serial ports, TV output, color LCD and camera interfaces).
- Direct support for high-level operating system such as Symbian™, Linux and WinCE® operating systems (OS).

1.5 Low power consumption

The new multimedia functionality of mobile products brings with it an increase in power consumption that is outpacing advances in battery technology. The STn8811A12 chip saves on power by avoiding the need for high clock speeds wherever possible, but its extremely low power consumption results from a systematic effort at all design levels to reduce power requirements. These include:

- The use of smart accelerators and distributed processing to off load from the CPU.
- Efficient code execution by means of innovative algorithms, energy-efficient instruction set architectures and Java acceleration.
- The efficient use of bandwidth for on-chip data transport, achieved by data compression, buffering and image scaling.
- Aggressive power management which includes turning off inactive parts of the chip and keeping the CPU in power-saving modes as much as possible.

1.6 Open platform strategy

The STn8811A12 is based around the MIPI™ software and hardware interface standard. This open platform strategy provides manufacturers with roadmap flexibility, allowing them to avoid becoming locked into a proprietary CPU architecture or vendor technology. This approach is facilitated by the following design points.

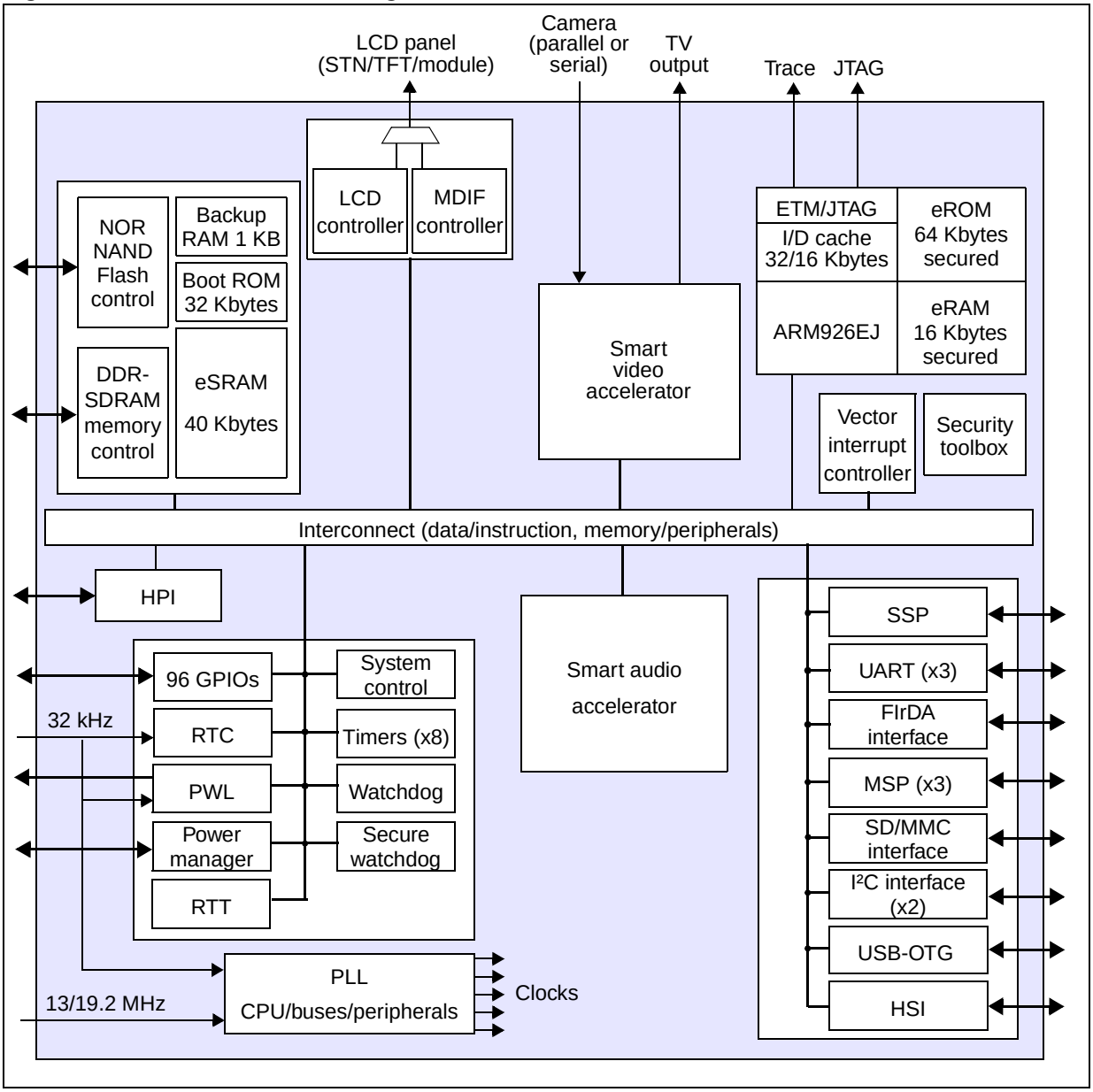
- The STn8811A12 employs the third-party ARM® processor which is the standard CPU for mobile devices, with industry-wide application support.
- Open, standard APIs are provided for the development of application code on a level which is abstracted from the physical hardware. This allows the development of multimedia plug-ins that are portable between products and which can be reused on future products without modification.
- The STn8811A12 offers a rich set of peripherals and the capability of adding new smart accelerators when required.
- The STn8811A12 enables best-in-class algorithm development on its smart accelerators.

2 Architecture overview

The STn8811A12 platform comprises an industry-standard ARM CPU supported by smart audio and video accelerators, on-chip memory and controllers, a rich set of peripheral interfaces, and a power management system. The processors, controllers, memory and peripheral interfaces are connected by a multi-layer advanced microcontroller bus architecture (AMBA) for efficient data transport between the components. The overall STn8811A12 architecture is illustrated in *Figure 2*.

The main hardware components of the STn8811A12 are listed and outlined in the sections below.

Figure 2. STn8811A12 block diagram



2.1 Smart video accelerator (SVA)

Using leading-edge technology, this block is a low-power, high-performance video accelerator that supports the following features:

- MPEG-4 simple profile level 0 codec video encoder and decoder; real time up to VGA 30 fps (encode only or decode only)
- H.263 profile 0 level 10 video codec; real time subQCIF or QCIF 15 fps for video-conferencing
- H.263 profile 0 level 30 video encoder or decoder; real-time up to CIF 30 fps
- JPEG baseline accelerated encoder or decoder, up to 4080 x 4080 pixels
- Programmable DSP (MMDSP+) for intermediate level processing, clocked at 66 MHz
- Picture pre-/post-processing
- Low-power implementation

2.2 Smart audio accelerator (SAA)

This high-performance block is a flexible sophisticated audio accelerator based on the MMDSP+ programmable audio DSP, clocked at 131 MHz, and features:

- 24-bit data path
- Ultra-low power implementation

The audio accelerator features:

- AAC, AAC+ (SBR) decoding, SBC, and more
- Speech codecs: AMR (WB, NB), and more
- Audio sample rates of 32 kHz, 44.1 kHz and 48 kHz
- Noise reduction and echo cancelling
- Stereo enhancements and surround effects

2.3 Advanced power management unit (PMU)

The dynamic PMU optimizes power consumption of the STn8811A12. It delivers all the platform clocks, and handles reset management. It also manages GPIO levels during sleep mode and emergency self-refresh of SDRAM.

The PMU controls the external voltage regulator, in order to change its settings in different modes. In deep-sleep mode, only GPIOs, the real-time clock (RTC), system and reset controller (SRC), PMU and secured RAM remain in operation. The PMU also controls the embedded 1.2 V voltage switch that switches off the logic supply after the platform has entered sleep mode.

The family of power manager ICs, STw481x companion chips, interface with the Nomadik STn8811A12 and optimize global system power consumption leveraging on the PMU.

2.4 ARM926EJ processor

The STn8811A12 CPU is an ARM926EJ reduced instruction set computer (RISC) processor. This 32-bit processor core supports 32-bit ARM® and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density.

The cached ARM CPU features a memory management unit (MMU) and is clocked at 393 MHz. It has a 32-Kbyte instruction cache and a 16-Kbyte data cache, and supports the Jazelle™ extensions for Java acceleration.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

2.5 Embedded memory units

- 32 Kbytes of public ROM (for boot purposes)
- 64 Kbytes of secured ROM (for security purposes)
- 40 Kbytes of public RAM
- 16 Kbytes of secured RAM (for security code and/or data)
- 1 Kbyte backup

2.6 Advanced security

The device contains 64 Kbytes of ROM and 16 Kbytes of RAM that are only accessible when the system is in a trusted environment. An advanced security framework enables M-commerce as well as authentication applications drawing on ST smartcard expertise:

- SHA-1/DES/3DES hardware accelerators
- True random number generator (RNG)
- Secured watchdog timer
- Unique die identification

2.7 Flexible static memory controller (FSMC)

The FSMC interfaces to off-chip multiplexed burst NOR Flash memory devices and NAND Flash memory devices, and to Compact Flash/CF+ cards. The FSMC manages up to 3 chip-selects of NOR Flash memories, and up to 2 chip-selects of NAND Flash memories or Compact Flash/CF+ devices. The memory controller features error code correction accelerated by hardware that reduces host CPU workload to support NAND Flash very fast read/write transfers.

2.8 SDRAM memory controller (SDMC)

The SDMC is used to interface with double-data rate SDRAM (DDR-SDRAM) at 131 MHz. The SDMC manages up to two chip-selects of 16-bit wide DDR-SDRAM. It can address up to 128 Mbytes (1 Gbits) of SDRAM.

2.9 Real time clock (RTC)

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

2.10 Timers

The STn8811A12 provides eight 16- or 32-bit (configurable) timers, as two groups of four. They generate the periodic and timed interrupts required by OS services.

2.11 Watchdog timer

This OS resource is used to trigger a system reset in the event of software failure.

2.12 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

2.13 System and reset controller (SRC)

The SRC provides a control interface for clock generation components external to the subsystem. It also controls system-wide and peripheral-specific energy management features.

2.14 Direct memory access (DMA) controllers

Direct memory accesses can be employed for data transfers involving DMA peripherals. A DMA controller services FIFO fill/empty requests from these peripherals immediately without CPU interaction. Peripheral-to-peripheral and memory-to-memory DMAs are also supported. A multichannel DMA controller is provided for efficient and concurrent data transfers.

2.15 Universal asynchronous receivers-transmitters (UARTs)

The STn8811A12 provides three autobaud UARTs, one of which offers all modem control/status signals. They are enhanced versions of the industry-standard 16C550 UART with a high data rate up to 3.692 Mbit/s.

2.16 Synchronous serial port (SSP)

The STn8811A12 provides one SSP for synchronous serial communication with external peripherals. SPI, MicroWire and T.I. protocols are supported, with programmable word length of up to 32 bits and data rate up to 24 Mbit/s.

The SSP has the following features in both master and slave configurations:

- Parallel-to-serial conversion of data written to an internal, 32-bit wide, 32-location deep, transmit FIFO
- Serial-to-parallel conversion of received data, which is buffered in a 32-bit wide, 32-location deep, receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and pre-scaler
- Programmable clock phase and polarity in SPI mode
- Support for direct memory accesses
- Support for several LCD smart panels

2.17 Camera interface

- Serial MIPI CSI camera interface, up to 416 Mbit/s data/strobe
- Parallel CCIR-656 camera interface, up to 66 MHz with embedded/external sync
- High resolution camera modules, up to 4 Mpixels

2.18 TV interface

The STn8811A12 interfaces with the Stw8009/STw8019 companion-chip, which performs YUV to RGB signal conversion and connects directly to a TV set.

2.19 Liquid crystal display controller (LCDC)

This interface drives LCD panels, and supports the following displays:

- STN displays: single- or dual-panel with 8-bit color and 4- or 8-bit monochrome
- TFT displays: 12-, 16-, 18- and 24-bit color

The resolution can be set as follows:

- 1-, 2- or 4-bits-per-pixel (bpp) palettized for mono STN
- 1-, 2-, 4- or 8-bpp palettized for color STN and TFT
- 16-bpp true-color non-palettized for color STN and TFT
- 24-bpp packed and non-packed true-color (non-palettized) for color TFT

2.20 Master display interface (MDIF)

This interface drives LCD display modules, that is, panels that include their own display memory and perform LCD panel refresh themselves. The MDIF is a parallel bidirectional interface that can send commands or data to or read data from the display panel logic. It has a DMA engine to automatically fetch data/commands from main memory without CPU intervention.

2.21 Pulse width light modulator (PWL)

The PWL provides control of LCD backlighting. It produces a series of pulses that are fed to the backlighting, where the width (or duty cycle) of the pulses determines the perceived lighting level. An 8-bit random sequence generator decreases the spectral power at the modulator harmonic frequencies.

2.22 General purpose inputs/outputs (GPIOs)

The STn8811A12 provides 96 programmable inputs or outputs that have switchable pull-up and pull-down resistors and are controllable in two modes:

- Software mode through an APB bus interface
- Hardware mode through a hardware control interface

The GPIO interface provides the following individually programmable functions:

- Any number of pins may be configured as interrupt sources
- Debouncing logic can be enabled for each GPIO to filter out glitches on I/Os
- Any GPIO may be used to wake up the device from sleep mode independent of interrupt programming, and the input level that triggers wake-up is definable for each enabled GPIO.

2.23 MultiMediaCard/secure data card interface (MMC/SD)

This interface can directly control one SD card (without encryption/decryption logic) or one MultiMediaCard. It also supports several of each card type using the GPIOs for card selection.

2.24 USB On-The-Go interface

The STn8811A12 USB interface is USB 2.0 compliant, with On-The-Go standard extension (rev 1.0) compliance. The USB-OTG features:

- Supports full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) signaling bit rate
- Supports session request protocol (SRP) and host negotiation protocol (HNP)
- 7 bidirectional endpoints plus control endpoint 0
- Digital interface to external PHY
- Fully compatible with STw4810 power manager companion chip

2.25 I²C bus interface

The STn8811A12 provides two I²C bus interfaces that support the following features:

- Slave transmitter/receiver and master transmitter/receiver modes
- Multi-master capability
- 10-bit addressing
- Standard (100 kHz) and fast (400 kHz) speeds
- Compliance with I²C and DDC standards

In addition to receiving and transmitting data, the interface converts data from serial to parallel format and vice-versa using an interrupt or polled handshake. The interrupts are enabled and disabled in software.

2.26 Fast IrDA interface (FIrDA)

This interface supports IrDA half-duplex communications. It performs modulation and demodulation of infrared signals, and the wrapping of IrLAP frames. The IrDA interface supports the following infrared modes and baud rates:

- Serial infrared (SIR): 9.6 Kbit/s, 19.2 Kbit/s, 38.4 Kbit/s, 57.6 Kbit/s and 115.2 Kbit/s
- Medium infrared (MIR): 576 Kbit/s and 1.152 Mbit/s
- Fast infrared (FIR): 4 Mbit/s

2.27 Multichannel serial ports (MSP)

The STn8811A12 provides three multichannel serial ports. These are synchronous receive and transmit serial interfaces that support a data rate of up to 48 Mbit/s with the following features:

- Philips I²S format: left aligned with one cycle between leading edge of frame synchronization and first data bit, 16 or 24 bits per sample
- Sony format: right aligned, 48 cycles per frame, 16 or 24 bits per sample
- Matsushita format: right aligned, 64 cycles per frame, 16 or 24 bits per sample
- Programmable number of bitclock cycles per frame: 32, 48 or 64
- Programmable polarity of bitclock and frame synchronization
- Programmable number of bits per sample: 16, 18, 20 or 24 bits

It also provides:

- µ-Law and A-Law compressing/expanding
- Independent framing and clocking for receive and transmit
- External shift clock or an internal, programmable frequency shift clock for data transfer
- Support for DMA transfers

2.28 High-speed serial interface (HSI)

The STn8811A12 includes a full-duplex high-speed serial interface (MIPI legacy HSI). This high-speed, 8-channel modem interface operates at up to 108 Mbit/s.

2.29 Host port interface (HPI)

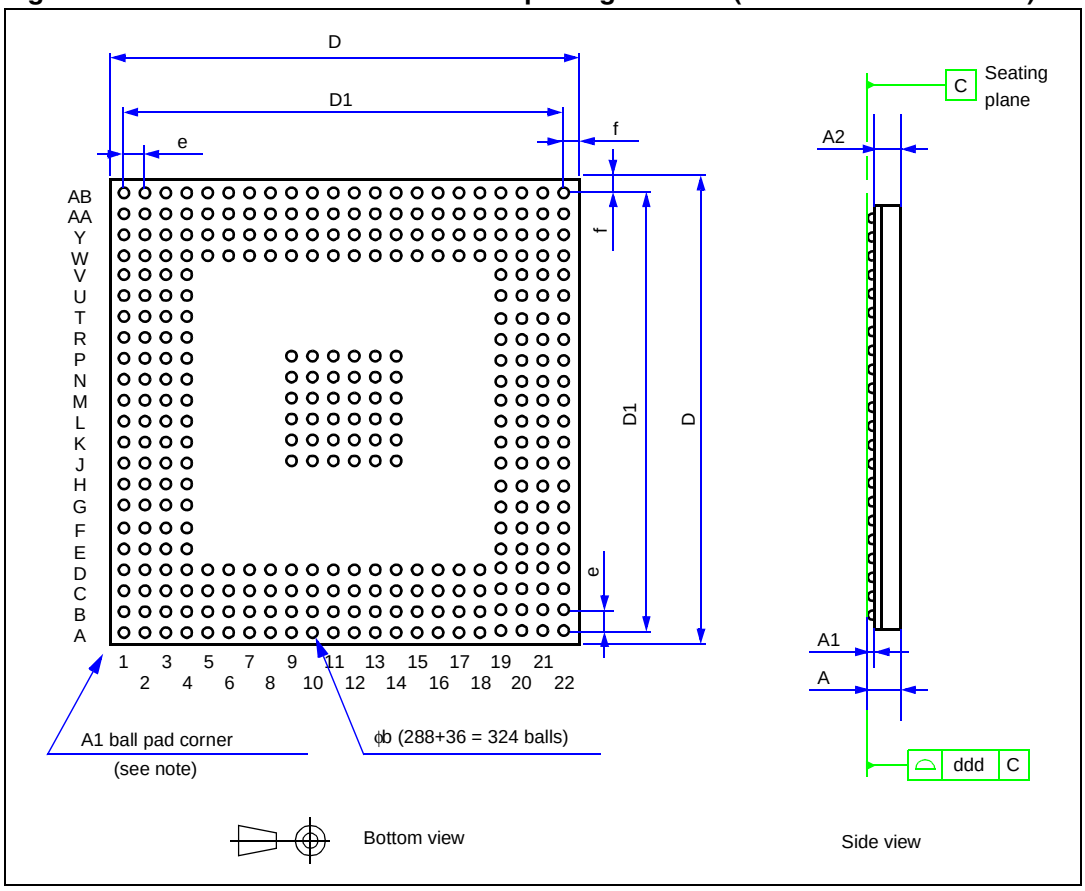
The host port interface features:

- 16-bit parallel data bus
- Multiplexed and non-multiplexed address/data bus
- Indirect host access
- Direct host access to a segment of STn8811A12 memory in multiplexed mode

3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 3. TFBGA 12 x 12 mm lead-free package outline (bottom and side views)



Note: The terminal A1 corner is identified on the top surface by using a corner chamfer, ink or metallized markings.

Table 1. Package dimensions

	Databook (mm)			Drawing (mm)		
Ref.	Min	Typ	Max	Min	Typ	Max
A	1.010	-	1.200	-	-	1.160(1)
A1	0.150	-	-	0.200	0.250	0.300
A2	-	0.820	-	-	0.820	-
b	0.250	0.300	0.350	0.250	0.300	0.350
D	11.750	12.000	12.150	11.900	12.000	12.100
D1	-	10.500	-	-	10.500	-
e	0.450	0.500	0.550	0.450	0.500	0.550
f	0.600	0.750	0.900	0.650	0.750	0.850
ddd	-	-	0.080	-	-	0.080

1. Maximum mounted height is 1.120 mm, based on a 0.28 mm ball pad diameter. Solder paste is 0.15 mm thick and 0.28 mm in diameter.

4 Ordering information

Table 2. Order codes

Part number	Package	Packing
STN8811B3A12HSBE	TFBGA 12mm x 12mm x 1.2mm	Tray

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
06-Jun-2007	1	Initial release.

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